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(57) **ABSTRACT**PCT Pub. Date: **Oct. 1, 2015**

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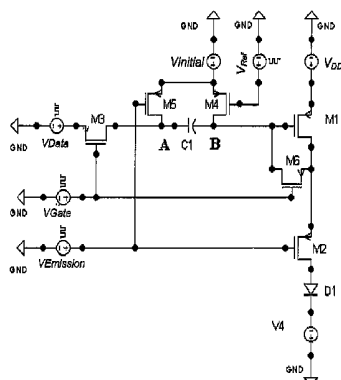
(51) **Int. Cl.**
G09G 3/32 (2016.01)

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CPC **G09G 3/3258** (2013.01); **G09G 3/3233**
(2013.01); **G09G 2300/0819** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC G09G 3/3233; G09G 3/3258; G09G
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2300/0861; G09G 2310/061; G09G
2310/08

See application file for complete search history.

13 Claims, 1 Drawing Sheet



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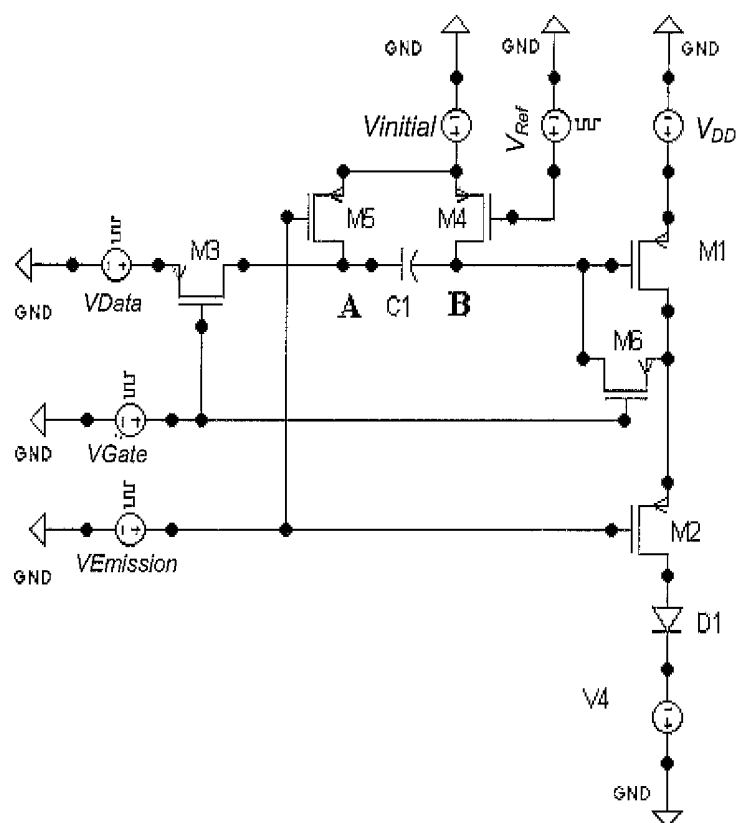


Fig. 1

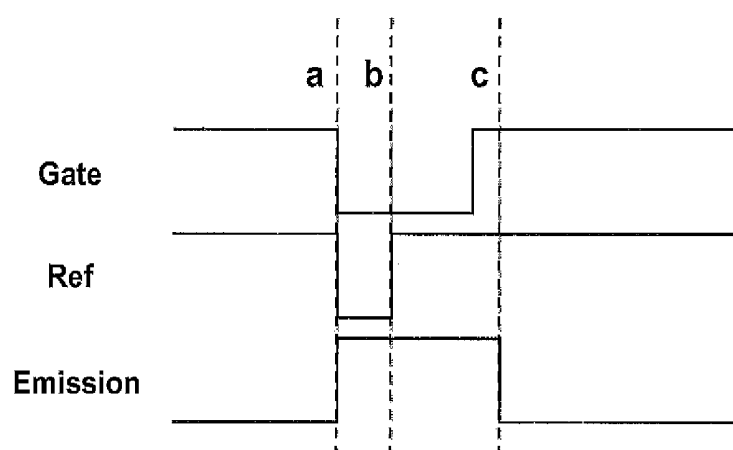


Fig. 2

PIXEL COMPENSATION CIRCUIT, ARRAY SUBSTRATE AND DISPLAY APPARATUS

CROSS REFERENCE TO RELATED APPLICATIONS

This application is the National Stage of PCT/CN2014/085320 filed on Aug. 27, 2014, which claims priority under 35 U.S.C. §119 of Chinese Application No. 201410111760.X filed on Mar. 24, 2014, the disclosure of which is incorporated by reference.

TECHNICAL FIELD

The present disclosure relates to a pixel compensation circuit, an array substrate, and a display apparatus.

BACKGROUND

Active matrix organic light emitting diode (AMOLED) display is a display technique applicable to a TV set and a mobile device, and has wide application prospect in power-sensitive portable electronic devices due to its characteristics of low power consumption, low cost and large size.

At present, in the AMOLED display field, in particular the large-size substrate design, a backplane thin film transistor (TFT) has non-uniformity and stability problems in the manufacturing process, which will not only cause threshold voltage offset due to non-uniformity of a driving OLED current, but also have the problem of TFT stability decrease after a long time of turning on bias voltage.

In the prior art, there are many AMOLED compensation circuit designs performed by only considering the problem of threshold voltage offset but neglecting the problem that load on a signal line will be increasing with the trend of the large-size AMOLED, thereby resulting in occurrence of voltage attenuation on the signal line, so as to influence the uniformity of current in the display area.

SUMMARY

In view of the deficiencies in the prior art, the present disclosure provides a pixel compensation circuit, an array substrate and a display apparatus, which not only has a function of compensating for the threshold voltage offset but also has a function of compensating for influence of signal voltage attenuation on current, and at the same time greatly reduces influence of signals from frame to frame

According to one aspect of the present disclosure, there is provided a pixel compensation circuit, comprising an organic light emitting diode, a driving transistor, first to fifth switch elements and a storage capacitor, wherein an anode of the organic light emitting diode is connected to a second terminal of the first switch element; a first terminal of the first switch element is connected to an output terminal of the driving transistor and a first terminal of the fifth switch element; a control terminal of the driving transistor is connected to a second terminal of the third switch element, a second terminal of the fifth switch element and a first terminal of the storage capacitor; and a second terminal of the storage capacitor is connected to a second terminal of the fourth switch element and a second terminal of the second switch element.

Alternatively, the pixel compensation circuit further comprises: a first driving voltage line connected to an input

terminal of the driving transistor; and a second driving voltage line connected to a cathode of the organic light emitting diode.

Alternatively, the pixel compensation circuit further comprises a data writing voltage line connected to a first terminal of the second switch element.

Alternatively, the pixel compensation circuit further comprises an initialization voltage line connected to a first terminal of the third switch element and a first terminal of the fourth switch element.

Alternatively, the pixel compensation circuit further comprises a writing switch signal line connected to a control terminal of the second switch element and a control terminal of the fifth switch element.

Alternatively, the pixel compensation circuit further comprises a resetting switch signal line connected to a control terminal of the third switch element.

Alternatively, the pixel compensation circuit further comprises a driving switch signal line connected to a control terminal of the first switch element and a control terminal of the fourth switch element.

As an example, both the driving transistor and the first to fifth switch elements can be thin film transistors.

According to another aspect of the present disclosure, there is provided an array substrate comprising any one of the above pixel compensation circuit.

According to another aspect of the present disclosure, there is provided a display apparatus comprising any one of the above array substrate.

The structure of the pixel compensation circuit of the present disclosure can make the current that finally drives OLED to emit light is unrelated with the threshold voltage V_{th} and the bias voltage V_{DD} . The pixel compensation circuit of the present disclosure can not only compensate OLED current deviation caused by the threshold voltage bias, but also has the function of compensating influence of signal voltage attenuation on current.

At the same time, such circuit structure further has a function of resetting the potential at the gate of the driving transistor from frame to frame, which guarantees to minimize the influence of an upper frame signal on a lower frame signal and greatly reduces the influence of a signal from frame to frame.

Of course, any product or method that implements the present disclosure does not necessarily need to realize the above all advantages simultaneously.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit structure diagram of a pixel compensation circuit in an embodiment of the present disclosure;

FIG. 2 is an operation timing diagram of a pixel compensation circuit in an embodiment of the present disclosure.

DETAILED DESCRIPTION

In order to make the purpose, technical solutions and advantages of embodiments of the present disclosure more clear, the technical solutions in the embodiments of the present disclosure will be described below clearly and completely by combining with the accompanying figures in the embodiments of the present disclosure. Apparently, the embodiments described below are a part of the embodiments of the present disclosure, but not all the embodiments. Based on the embodiments in the present disclosure, all the other

embodiments obtained by those skilled in the art without paying any inventive word belong to the protection scope of the present disclosure.

First Embodiment

There provides in an embodiment of the present disclosure a pixel compensation circuit. As shown in FIG. 1, the circuit comprises: an organic light emitting diode D1, a driving transistor M1, first to fifth switch elements M2 to M6 and a storage capacitor C1.

In the circuit as shown in FIG. 1, an anode of the organic light emitting diode D1 is connected to a second terminal of the first switch element M2. A first terminal of the first switch element M2 is connected to a second terminal (output terminal) of the driving transistor M1 and a first terminal of the fifth switch element M6.

A control terminal of the driving transistor M1 is connected to a second terminal of the third switch element M4, a second terminal of the fifth switch element M6 and a first terminal (corresponding to node B in FIG. 1) of the storage capacitor C1.

A second terminal of the storage capacitor C1 is connected to a second terminal of the fourth switch transistor M5 and a second terminal (corresponding to node A in FIG. 1) of the second switch element M3.

Herein, the switch elements refer to elements whose first terminal and second terminal are controlled by a signal of the control terminal whether or not to be connected. Of course, the switch elements can be implemented by a variety of specific electrical elements.

Thus, this circuit has the basic construction and connecting relationships as described above, wherein the driving transistor M1, the first switch element M2 (which can be regarded as a conducting wire when it is turned on) and the organic light emitting diode D1 constitute the basic OLED driving relationship, while the first to fifth switch elements can be controlled by signals at their respective control terminals to be in a turn-on/turn-off state respectively.

Further, in order to realize the functions of the circuit, it needs to apply necessary bias in the circuit. For this reason, the circuit further comprises:

a first driving voltage line, applied thereto a positive operating bias voltage V_{DD} , and connected to a first terminal (input terminal) of the driving transistor M1;

a second driving voltage line, applied thereto a negative operating bias voltage V_4 , and connected to a cathode of the organic light emitting diode D1;

a data writing voltage line, applied thereto a data writing voltage VData that sets how the OLED in the circuit emits light, and connected to a first terminal of the second switch element M3; and

an initialization voltage line, applied thereto a constant initialization voltage Vinitial, and connected to a first terminal of the third switch element M4 and a first terminal of the fourth switch element M5.

Furthermore, three signal lines are adopted herein to control turn-on or turn-off of each switch element respectively. That is, the circuit further comprises:

a writing switch signal line, applied thereto a writing switch signal voltage VGate, and connected to a control terminal of the second switch element M3 and a control terminal of the fifth switch element M6;

a resetting switch signal line, applied thereto a resetting switch signal voltage VRef, and connected to the control terminal of the third switch element M4; and

a driving switch signal line, applied there to a driving switch signal voltage VEmission, and connected to a control terminal of the first switch element M2 and a control terminal of the fourth switch element M5.

Of course, the zero point of potential of all bias voltages is connected to a same common terminal, and the zero point of potential of all signal voltages is also connected to a same common terminal.

Alternatively, the driving transistor and the first to fifth switch elements are all thin film transistors TFTs.

By corresponding to the above feature, the first terminal (input terminal) of the driving transistor and the first terminals of the first to fifth switch elements represent sources, the second terminal (output terminal) of the driving transistor and the second terminals of the first to fifth switch elements represent drains, and the control terminal of the driving transistor and the control terminals of the first to fifth switch transistors represent gates. Further, TFTs adopted in the present embodiment are P channel type thin film transistors.

Since the pixel compensation circuit in the embodiment comprises six TFTs and one capacitor, it can be called as a new type 6T1C pixel compensation circuit according to the common naming way in the art.

Based on the circuit connection under the above conditions, the operation principle of the circuit can be described as follows:

FIG. 2 shows an operation timing diagram of the circuit. As shown in FIG. 2, Gate, Ref, Emission represent a writing switch signal, a resetting switch signal, and a driving switch signal respectively. In general, the operation of the circuit is divided into three phases: a resetting phase (a-b), a data writing and threshold voltage latching phase (b-c) and a light emitting phase (c-).

In the resetting phase (a-b), Ref and Gate are at a low level. Since Gate is at the low level, the transistors M3 and M6 are turned on. The turn-on of M3 makes the potential at node A of the storage capacitor C1 become VData, while the turn-on of M6 connects the gate and drain of the driving transistor M1, so that M1 forms a diode connection and is in the turn-on state. At this time, since Ref is also at the low level, the transistor M4 is turned on. Now, a loop composed of the transistors M1, M6 and M4 will be formed.

Thus, in resetting phase, node B of the storage capacitor C1 connected to the loop is controlled by the circuit of M4, M1 and M6. Since M4 is directly connected to a power supply signal, so that a signal at node B is controlled by M4 instead of by the loop of M1 and M6. Therefore, at this time, the potential at node B is Vinitial potential. In the resetting phase of each frame, the node B will be reset to the Vinitial potential. The potential of node A at the other terminal of the storage capacitor is controlled by M3. At this time, VData is directly loaded. Therefore, in the resetting phase, the potentials at the terminals A and B of the storage capacitor will be stabilized at VData and Vinitial respectively.

In the data writing and threshold voltage latching phase (b-c), Ref is at a high level, so that M4 is turned off and the node B is controlled only by the loop of M1 and M6. At this time, M1 is still in the diode connecting mode. Therefore, the potential at node B is written a sum of V_{DD} and the threshold voltage V_{th} , while the potential at node A is also directly loaded VData by M3. When this phase ends, the potentials at the two terminals A and B of the storage capacitor are VData and $V_{DD}+V_{th}$ respectively.

In the light emitting phase, Gate is at the high level, and thus the transistors M3 and M6 are turned off. The Emission signal is at the low level, and thus the transistors M5 and M2 are turned on. The turn-on of M5 makes the potential of node

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A at one terminal of the storage capacitor C1 become Vinitial. According to the principle of capacitive charge conservation, the potential at node B becomes Vinitial+V_{DD}+V_{th}-VData, i.e., making the gate signal of the driving transistor M1 become Vinitial+V_{DD}+V_{th}-VData. Since M1 operates in a saturation region, it can be known according to the current formula in the saturation region of transistors:

$$\begin{aligned} I_{DS} &= \frac{1}{2} K (V_{GS} - V_{th})^2 \\ &= \frac{1}{2} K (V_{initial} + V_{DD} + V_{th} - V_{Data} - V_{DD} - V_{th})^2 \\ &= \frac{1}{2} K (V_{initial} - V_{Data})^2 \end{aligned}$$

where K in the same structure is relatively stable, and can be regarded as a constant.

Therefore, in the process that OLED emits light, the current flowing through the organic light emitting diode connected to the drain of the driving transistor M1 is only related to Vinitial and VData signals, but is unrelated to V_{th} and V_{DD}. Since Vinitial will not form a current loop, the influence of Vinitial IR Drop (voltage drop, i.e., the voltage attenuation on the signal line as mentioned in the background of the present disclosure) does not exist. Thus, the problem of non-uniformity of current flowing through OLED due to non-uniformity of V_{th} caused by the back-plane manufacturing process will not occur and the problem of non-uniformity of light emitting will not be caused either. At the same time, the potential at node A of the storage capacitor is always the Vinitial signal in the process of emitting light, and thus no charge loss occurs, which ensures the stability of the potential at node B so that the current of M1 is stable and thus the organic light emitting diode emits light stably.

Of course, the above embodiment is just used for describing the principle of the present disclosure, but not used for limiting the present disclosure. Although the present disclosure has been described in detail by referring to the above embodiments, those skilled in the art shall understand: no matter what kind of voltage bias is adopted, what kind of control line is adopted to control connection or what kind of specific switches, capacitors and transistor elements are adopted in the specific implementation processes, it can be implemented by referring to the operation principle described in the embodiments of the present disclosure, without departing from the spirit and scope of the technical solutions in the respective embodiments of the present disclosure.

Second Embodiment

Based on the same inventive concept, there further provides an embodiment of the present disclosure an array substrate comprising any one of the above pixel compensation circuit. Since the array substrate provided in the embodiments of the present disclosure has the same technical features as any one of the above pixel compensation circuits, it can solve the same technical problems and produce the same technical effects.

Third Embodiment

Based on the same inventive concept, there further provides in an embodiment of the present disclosure a display

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apparatus comprising any one of the array substrates. The display apparatus can be any product or components having a display function, such as an electronic paper, an OLED panel, a mobile phone, a tablet computer, a TV set, a display, a notebook computer, a digital photo frame, and a navigator and so on.

Since the display apparatus provided in the embodiment of the present disclosure has the same technical features as any one of the above array substrates, it can solve the same technical problems and produce the same technical effects.

To sum up, the pixel compensation circuit, the array substrate and the display apparatus provided in the present disclosure can not only compensate for OLED current deviation caused by the threshold voltage offset, but also have the function of compensating for the influence of signal voltage attenuation on current.

At the same time, such circuit structure further has a function of resetting the potential at the gate of the driving TFT from frame to frame, which ensures to minimize the influence of an upper frame signal on a lower frame signal and greatly reduces the influence of signals from frame to frame.

The above embodiments are just used for describing the technical solutions of the present disclosure, but not used for limiting the technical solutions of the present disclosure. Although the embodiments of the present disclosure have been described in detail by referring to the embodiments as described above, those skilled in the art shall understand: the technical solutions disclosed in the above embodiments can be amended, or a part of technical features can be replaced by equivalent technical features. And these amendments or replacements do not depart from the spirit and scope of the present disclosure defined in the Claims.

The present application claims a priority of a Chinese patent application No. 201410111760.X filed on Mar. 24, 2014. The content disclosed by the Chinese patent application is incorporated by reference herein in full as a part of the present disclosure.

What is claimed is:

1. A pixel compensation circuit, comprising an organic light emitting diode, a driving transistor, first to fifth switch elements and a storage capacitor, wherein:

an anode of the organic light emitting diode is connected to a second terminal of the first switch element;

a first terminal of the first switch element is connected to an output terminal of the driving transistor and a first terminal of the fifth switch element;

a control terminal of the driving transistor is connected to a second terminal of the third switch element, a second terminal of the fifth switch element and a first terminal of the storage capacitor;

a second terminal of the storage capacitor is connected to a second terminal of the fourth switch element and a second terminal of the second switch element;

the pixel compensation circuit further comprises a driving switch signal line connected to a control terminal of the first switch element and a control terminal of the fourth switch element;

the pixel compensation circuit further comprises a data writing voltage line connected to a first terminal of the second switch element;

wherein a first terminal of the third switch element is connected to a first terminal of the fourth switch element.

2. The pixel compensation circuit according to claim 1, wherein it further comprises:

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a first driving voltage line connected to an input terminal of the driving transistor; and
a second driving voltage line connected to a cathode of the organic light emitting diode.

3. The pixel compensation circuit according to claim 1, wherein it further comprises: an initialization voltage line connected to the first terminal of the third switch element and the first terminal of the fourth switch element.

4. The pixel compensation circuit according to claim 1, wherein it further comprises: a writing switch signal line connected to a control terminal of the second switch element and a control terminal of the fifth switch element.

5. The pixel compensation circuit according to claim 1, wherein it further comprises: a resetting switch signal line connected to a control terminal of the third switch element.

6. The pixel compensation circuit according to claim 1, wherein the driving transistor and the first to fifth switch elements are thin film transistors.

7. An array substrate comprising the pixel compensation circuit according to claim 1.

8. A display apparatus comprising the array substrate according to claim 7.

9. The array substrate according to claim 7, wherein the pixel compensation circuit further comprises:

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a first driving voltage line connected to an input terminal of the driving transistor; and

a second driving voltage line connected to a cathode of the organic light emitting diode.

10. The array substrate according to claim 7, wherein pixel compensation circuit further comprises: an initialization voltage line connected to the first terminal of the third switch element and the first terminal of the fourth switch element.

11. The array substrate according to claim 7, wherein pixel compensation circuit further comprises: a writing switch signal line connected to a control terminal of the second switch element and a control terminal of the fifth switch element.

12. The array substrate according to claim 7, wherein pixel compensation circuit further comprises: a resetting switch signal line connected to a control terminal of the third switch element.

13. The array substrate according to claim 7, wherein, in the pixel compensation circuit, the driving transistor and the first to fifth switch elements are thin film transistors.

* * * * *

专利名称(译)	像素补偿电路，阵列基板和显示装置		
公开(公告)号	US9564081	公开(公告)日	2017-02-07
申请号	US14/436208	申请日	2014-08-27
[标]申请(专利权)人(译)	京东方科技集团股份有限公司		
申请(专利权)人(译)	京东方科技集团股份有限公司.		
当前申请(专利权)人(译)	京东方科技集团股份有限公司.		
[标]发明人	MA ZHANJIE		
发明人	MA, ZHANJIE		
IPC分类号	G09G3/32 G09G3/3233		
CPC分类号	G09G3/3258 G09G3/3233 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2310/061 G09G2310/08 G09G2320/0223		
优先权	201410111760.X 2014-03-24 CN		
其他公开文献	US20160180772A1		
外部链接	Espacenet USPTO		

摘要(译)

提供了像素补偿电路，阵列基板和显示装置。像素补偿电路包括有机发光二极管 (D1)，驱动晶体管 (M1)，第一至第五开关元件 (M2-M5) 和存储电容器 (C1)，其中有有机发光二极管的阳极 (D1a) 是连接到第一开关元件的第二端子 (M2b)；第一开关元件的第一端子 (M2a) 连接到驱动晶体管 (M1) 的输出端子和第五开关元件的第一端子 (M5a)；一个驱动晶体管 (M1) 的控制端子连接到第三开关元件的第二端子 (M4b)，第五开关元件的第二端子 (M5b) 和存储电容器的第一端子 (C1a)；存储电容器的第二端子 (C1b) 连接到第四开关元件的第二端子 (M3b) 和第二开关元件的第二端子 (M3b)。像素补偿电路不仅具有补偿阈值电压偏移的功能，还具有补偿信号电压衰减影响的功能。当前。

